ABSTRACT

Apparatus for use in a computer system comprises a bus architecture, a plurality of modules connected to the bus architecture, at least one module being latency tolerant and at least one module being latency intolerant. The bus architecture comprises a primary bus (3) having latency intolerant modules connected thereto, a secondary bus (4) having latency tolerant modules connected thereto, and a primary to secondary bus interface module (5) interconnecting the primary and secondary buses.